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CORP., MATROX TECH, INC. and AEROFLEX COLORADO
SPRINGS. INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, et al., Defendants.	Case No. C03-04669 MJJ (EMC) Case No. C03-2289 MJJ (EMC) **DECLARATION OF ERIK OLSON IN SUPPORT OF DEFENDANTS' NOTICE OF MOTION AND MOTION FOR SUMMARY JUDGMENT OF NONINFRINGEMENT UNDER 35 U.S.C. §271(g)**
SYNOPSYS, INC., Plaintiff, vs. RICOH COMPANY, LTD., Defendant.	Date: August 9, 2005 Time: 9:30 a.m. Courtroom: 11, 19th Floor Judge: Martin J. Jenkins

I, Erik Olson, declare as follows:

1. I am a Director of Applications Consulting at Synopsys, Inc. ("Synopsys") specializing in physical implementation engagements—sometimes known as "back end" design. I have been an employee of Synopsys since August 12, 1991. I have been involved in the design of ASICs since 1989. I have two bachelors degrees, one in Computer Science and one in Computer Engineering, from University of Minnesota. I make this Declaration of my personal knowledge, and if called as a witness, I could and would testify competently to the statements contained herein.

2. The process of designing ASICs includes many steps. Because the design process itself has many hand offs, it is common to divide the design implementation process into at least two major portions: "front end" and "back end" design. In many cases, these two portions are performed by different companies and in some cases, even more than two. Even if done by a single company, in the majority of such cases it is done by completely different groups of people with very different skills and training. The end result of the overall design process is a mask data file that can be used—frequently by companies other than the designer—for photomask manufacturing processes.

3. The "front end" design steps for a circuit include the high level steps of:

i.) identification of functions to be performed by the new ASIC and preparation of design specifications identifying those functions;
ii.) design capture of logic to implement the functional specification (e.g. by describing the logic in textual Verilog, or VHDL, descriptions);
iii.) verification of the functionality of the captured description;
iv.) synthesis of the description into a netlist; and
v.) netlist verification.

4. The "back end" design steps for a circuit include the high level steps of:

i.) generating the design information known as physical layout using software for placement and routing of the components and their interconnections;
ii.) verification of the physical layout with the software processes used for timing characterization, design rule checking, etc.; and
iii.) generation of mask data from the physical layout.

5. The generation of a netlist is included in step 3(iv) above. I understand that the Court has defined a netlist as "a description of the hardware components (and their interconnections) needed to manufacture the ASIC as used by subsequent processes, e.g., mask development, foundry, etc."

6. Preparation of mask data from the netlist follows the high level steps described above (step 3(v) followed by steps 4(i)-(iii)). Mask data is a set of instructions used by electron beam equipment to make photomasks (the process of generating mask data is also referred to as "fracturing").

7. There are many more detailed steps that take place in transforming a netlist (output of step 3(iv)) into mask data (output of step 4(iii)). These steps include:

a) netlist verification:

(Part 1) Netlist verification checks that the netlist output by step 3(iv) matches the functional description provided by the user and

(Part 2) Netlist verification checks that the netlist output meets the design constraints, e.g. timing, area, power consumption, etc.

Users typically would use Synopsys tools such as Formality, Primetime, and VCS for these sub-steps. Throughout this declaration I am addressing the Synopsys products that I consider most relevant to the step being discussed; however, for many of these steps competitor software companies offer tools that provide similar functionality.

b) design planning: Sometimes referred to as floorplanning, design planning has three main parts:

(Part 1) Design planning performs an overall floor plan for the placement of the functional units of the chip, sometimes called "rough placement", and checks the timing and top level routing between those functional units;

(Part 2) Design planning designs and routes the electrical power grid, including the placement of power and ground wiring;

(Part 3) Design planning defines the pin positions for the inputs and outputs of the chip.

Users can use one or more Synopsys tools such as Astro, IC Compiler, and JupiterXT for this step.

c) physical implementation: Physical implementation has three main parts:

(Part 1) Placement defines a physical location in two dimensional space for the position of each component in the netlist;

(Part 2) Clock tree design, sometimes called clock tree synthesis, creates and defines the distribution of the previously defined clock signal (e.g. from the clock defined in the previously input textual Verilog, or VHDL, descriptions) into the placed components of the netlist; and

(Part 3) Interconnect routing provides the electrical connections between the placed components—according to the connections defined in the netlist.

Users can use one or more Synopsys tools such as Astro and IC Compiler for this step.

d) extraction and analysis:

(Part 1) Extraction comprises the extraction of electrical characteristics of the interconnect components from the physical layout (created in the routing step above) to produce a file for further analysis.

(Part 2) Analysis comprises both the review of the electrical characteristics file and the physical layout itself to confirm that the design constraints are met, e.g. timing, area, power grid analysis (IR Drop, voltage drop), power consumption, etc.

Users can use one or more Synopsys tools such as AstroRail, PrimeRail, Primetime, and StarRC/XT for this step.

e) physical verification: Physical verification verifies the physical layout with other software processes such as those for design rule checking, layout-versus-schematic, etc. Users can use the Synopsys Hercules tool for this step.

f) resolution enhancement: Resolution enhancement uses software to perform geometric manipulations to the physical layout to improve manufacturability. Users can use one or more Synopsys tools such as Proteus, ProteusAF, and PSMGen for this step.

g) mask data preparation: Sometimes called fracturing, mask data preparation is the conversion of the physical layout into the instructions used by the electron beam machines to make the photomasks. Users can use the Synopsys CATS tool for this step.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. This declaration was executed in Bellevue, Washington on June 14, 2005.

Erik Olson